Amendments to the Claims:

All claims have been amended herein. Claim 23 is canceled without prejudice or disclaimer. Please note that all claims currently pending and under consideration in the referenced application are shown below. Please enter these claims as amended. This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1. (Currently Amended) A method of forming a microelectronic structure, the method comprising:

forming an oxide layer upon a semiconductor substrate;

forming a first dielectric layer upon ~~said~~the oxide layer;

selectively removing ~~said~~the first dielectric layer to expose ~~said~~the oxide layer at a plurality of areas;

forming a second dielectric layer over ~~said~~the oxide layer and ~~said~~the first dielectric layer, wherein ~~said~~the forming a second dielectric layer includes forming a second dielectric layer over and in contact with the exposed oxide layer at ~~said~~the plurality of areas;

selectively removing ~~said~~the second dielectric layer to form a plurality of spacers from ~~said~~the second dielectric layer, wherein each ~~said~~ spacer is situated upon ~~said~~the oxide layer, is in contact with ~~said~~the first dielectric layer, and is adjacent to an area of ~~said~~the plurality of areas;

forming a plurality of isolation trenches extending below ~~said~~the oxide layer into ~~said~~the semiconductor substrate, wherein each ~~said~~ isolation trench is adjacent to and below a pair of ~~said~~the spacers and is situated at a corresponding area of ~~said~~the plurality of areas, and wherein each isolation trench has a top edge;

forming a liner upon a sidewall of each ~~said~~ isolation trench;

filling each~~-said~~ isolation trench with a conformal layer, ~~said~~the conformal layer extending above ~~said~~the oxide layer in contact with a corresponding pair of ~~said~~the spacers, wherein ~~said~~the filling is performed by depositing ~~said~~the conformal layer, and ~~said~~the depositing is carried out to the extent of filling each ~~said~~ isolation trench and extending over ~~said~~the spacers and over ~~said~~the first dielectric layer so as to define an upper surface contour of the conformal layer; and

directly planarizing the conformal layer beginning with the upper surface contour of the conformal layer and extending at least to the first dielectric layer and each ~~said~~ spacer to form therefrom an upper surface for each ~~said~~ isolation trench that is co-planar to the other upper surfaces;

wherein the conformal layer comprises a material that is electrically insulative and extends continuously between and within ~~said~~the plurality of isolation trenches.

2. (Canceled).

3. (Currently Amended) ~~A method~~The method according to Claim 1, wherein ~~said~~the liner is a thermally grown oxide of ~~said~~the semiconductor substrate.

4. (Currently Amended) ~~A method~~The method according to Claim 1, wherein forming ~~said~~the liner upon ~~said~~the sidewall of ~~said~~the isolation trench comprises deposition of a composition of matter.

5. (Currently Amended) ~~A method~~The method according to Claim 1, further comprising forming a doped region below the termination of each ~~said~~the isolation trench within ~~said~~the semiconductor substrate.

6. (Currently Amended) ~~A method~~The method according to Claim 1, wherein ~~said~~the upper surface for each ~~said~~the isolation trench is formed by chemical mechanical planarization.

7. (Currently Amended) A method of forming a microelectronic structure, the method comprising:

forming an oxide layer upon a semiconductor substrate;

forming a first dielectric layer upon ~~said~~the oxide layer;

selectively removing ~~said~~the first dielectric layer to expose ~~said~~the oxide layer at a plurality of areas;

forming a second dielectric layer over ~~said~~the oxide layer and ~~said~~the first dielectric layer, wherein ~~said~~the forming a second dielectric layer includes forming a second dielectric layer on and in contact with the exposed oxide layer at ~~said~~the plurality of areas;

selectively removing ~~said~~the second dielectric layer to form a plurality of spacers from ~~said~~the second dielectric layer, wherein each ~~said~~the spacer is situated upon ~~said~~the oxide layer, is in contact with ~~said~~the first dielectric layer, and is adjacent to an area of ~~said~~the plurality of areas;

forming a plurality of isolation trenches extending below ~~said~~the oxide layer into ~~said~~the semiconductor substrate, wherein each ~~said~~ isolation trench is adjacent to and below a pair of ~~said~~the spacers and is situated at a corresponding area of ~~said~~the plurality of areas, and wherein each isolation trench has an edge;

rounding the top edge of each of ~~said~~the isolation trenches;

filling each ~~said~~ isolation trench with a conformal layer, ~~said~~the conformal layer extending above ~~said~~the oxide layer in contact with a corresponding pair of ~~said~~the spacers, wherein ~~said~~ filling is performed by depositing ~~said~~the conformal layer and ~~said~~ depositing is carried out to the extent of filling each ~~said~~ isolation trench and extending over ~~said~~the spacers and over ~~said~~the first dielectric layer to a first thickness of the conformal layer relative to ~~said~~the spacers and ~~said~~the first dielectric layer;

planarizing the first thickness of the conformal layer to a second reduced thickness in a single-step to form therefrom an upper surface for each ~~said~~ isolation trench that is co planar to the other upper surfaces, wherein:

the conformal layer comprises a material that is electrically insulative and extends continuously between and within ~~said~~the plurality of isolation trenches;

~~said~~the conformal layer and ~~said~~the spacers form ~~said~~the upper surface for each ~~said~~ isolation trench, each ~~said~~the upper surface being formed from ~~said~~the conformal layer and ~~said~~the spacer and being situated above ~~said~~the oxide layer; and

~~said~~the first dielectric layer is in contact with at least a pair of ~~said~~the spacers and ~~said~~the oxide layer.

8. (Currently Amended) ~~A method~~The method according to Claim 7, further comprising:

removing ~~said~~the oxide layer upon a portion of a surface of ~~said~~the semiconductor substrate; and

forming a gate oxide layer upon ~~said~~the portion of ~~said~~the surface of ~~said~~the semiconductor substrate.

9. (Currently Amended) ~~A method~~The method according to Claim 7, further comprising ~~wherein said upper surface for each said isolation trench is formed in an etch process~~ removing the first dielectric layer using an etch recipe that etches ~~said~~the first dielectric layer faster than ~~said~~the conformal layer and ~~said~~ the spacers by a ratio in a range from about 1:1 to about 2:1.

10. (Currently Amended) ~~A method~~The method according to Claim 9, wherein ~~said~~the ratio is in a range from about 1.3:1 to about 1.7:1.

11. (Currently Amended) ~~A method~~The method according to Claim 7, wherein ~~said~~the upper surface for each ~~said~~the isolation trench is formed by the steps comprising:

chemical mechanical planarization, wherein ~~said~~the conformal layer, ~~said~~the spacers, and ~~said~~the first dielectric layer form a planar first upper surface; and

an etch that forms a second upper surface, ~~said~~the second upper surface being situated above ~~said~~the pad oxide layer.

12. (Currently Amended) ~~A method~~The method according to Claim 11, wherein ~~said~~the etch uses an etch recipe that etches ~~said~~the first dielectric layer faster than said conformal layer and said spacers by a ratio in a range from about 1:1 to about 2:1.

13. (Currently Amended) ~~A method~~The method according to Claim 12, wherein ~~said~~the ratio is in a range from about 1.3:1 to about 1.7:1.

14. (Currently Amended) A method of forming a microelectronic structure, the method comprising:

forming an oxide layer upon a semiconductor substrate;

forming a silicon nitride layer upon ~~said~~the oxide layer;

selectively removing ~~said~~the silicon nitride layer to expose ~~said~~the oxide layer at a plurality of areas;

forming a first silicon dioxide layer over ~~said~~the oxide layer and over ~~said~~the silicon nitride layer, wherein ~~said~~ forming a first silicon dioxide layer includes forming a first silicon dioxide layer on and in contact with the exposed oxide layer at ~~said~~the plurality of areas;

selectively removing ~~said~~the first silicon dioxide layer to form a plurality of spacers from ~~said~~the first silicon dioxide layer, wherein each ~~said~~ spacer is situated upon ~~said~~the oxide layer, is contact with ~~said~~the silicon nitride layer, and is adjacent to an area of ~~said~~the plurality of areas;

forming a plurality of isolation trenches extending below ~~said~~the oxide layer into and terminating within ~~said~~the semiconductor substrate, wherein each ~~said~~ isolation trench is adjacent to and below a pair of ~~said~~the spacers and is situated at a corresponding area of ~~said~~the plurality of areas, and wherein each isolation trench has a top edge;

forming a corresponding electrically active region below the termination of each ~~said~~ isolation trench within ~~said~~the semiconductor substrate;

forming a liner upon a sidewall of each ~~said~~ isolation trench, ~~said~~the liner being confined preferentially within each ~~said~~ isolation trench and extending from an interface thereof with ~~said~~the oxide layer to the termination of ~~said~~the isolation trench within ~~said~~the semiconductor substrate;

filling each ~~said~~ isolation trench with a conformal second silicon dioxide layer, ~~said~~the conformal second silicon dioxide layer within each ~~said~~ isolation trench extending above ~~said~~the oxide layer in contact with the corresponding pair of ~~said~~the spacers, wherein ~~said~~ filling is performed by depositing ~~said~~the conformal second silicon dioxide layer, and ~~said~~ depositing is carried out to the extent of filling each ~~said~~ isolation trench and extending over ~~said~~the spacers and ~~said~~the silicon nitride layer; and

selectively removing ~~said~~the conformal second silicon dioxide layer and ~~said~~the spacers to form an upper surface for each ~~said~~ isolation trench that is co-planar to the other ~~said~~ upper surfaces and being situated above ~~said~~the pad oxide layer, wherein a material that is electrically insulative extends continuously between and within ~~said~~the plurality of isolation trenches, and wherein ~~said~~ selectively removing is performed directly on the conformal second silicon dioxide layer and in the absence of masking the conformal second silicon dioxide layer over each ~~said~~ isolation trench.

15. (Currently Amended) ~~A method~~The method according to Claim 14, wherein ~~said~~the a liner is a thermally grown oxide of ~~said~~the semiconductor substrate.

16. (Currently Amended) ~~A method~~The method according to Claim 14, wherein ~~said~~the liner is composed of silicon nitride.

17. (Currently Amended) ~~A method~~The method according to Claim 15, further comprising:

removing ~~said~~the oxide layer upon a portion of a surface of ~~said~~the semiconductor substrate; and

forming a gate oxide layer upon ~~said~~the portion of ~~said~~the surface of ~~said~~the semiconductor substrate.

18. (Currently Amended) A method of forming a microelectronic structure, the method comprising:

forming an oxide layer upon a semiconductor substrate;

forming a polysilicon layer upon ~~said~~the oxide layer;

forming a first dielectric layer upon ~~said~~the polysilicon layer;

selectively removing ~~said~~the first dielectric layer and ~~said~~the polysilicon layer to expose ~~said~~the oxide layer at a plurality of areas;

forming a second dielectric layer conformally over ~~said~~the oxide layer, ~~said~~the polysilicon layer, and ~~said~~the first dielectric layer, wherein ~~said~~the forming a second dielectric layer includes forming a second dielectric layer on and in contact with the exposed oxide layer at ~~said~~the plurality of areas;

selectively removing ~~said~~the second dielectric layer to form a plurality of spacers from ~~said~~the second dielectric layer, wherein each ~~said~~the spacer is upon ~~said~~the oxide layer, is in contact with both ~~said~~the polysilicon layer and ~~said~~the first dielectric layer, and is adjacent to an area of ~~said~~the plurality of areas;

forming a plurality of isolation trenches extending below ~~said~~the oxide layer and from top edges into and terminating within ~~said~~the semiconductor substrate, wherein each ~~said~~ isolation trench is adjacent to and below a pair of ~~said~~the spacers and is situated at a corresponding area of ~~said~~the plurality of areas;

rounding the top edges of each of ~~said~~the isolation trenches;

filling each ~~said~~ isolation trench with a conformal third layer, ~~said~~the conformal third layer extending above ~~said~~the oxide layer in contact with a corresponding pair of ~~said~~the spacers, wherein ~~said~~ filling is performed by depositing ~~said~~the conformal third layer, and ~~said~~ depositing is carried out to the extent of filling each ~~said~~ isolation trench and extending over ~~said~~the spacers and over ~~said~~the first dielectric layer;

planarizing the conformal third layer to form therefrom an upper surface for each said isolation trench that is co-planar to the other said upper surfaces comprising directly planarizing the conformal third layer and each of the spacers to form therefrom the co-planar upper surfaces in the absence of masking the conformal third layer over each of the isolation trenches;

wherein a material that is electrically insulative extends continuously between and within ~~said~~the plurality of isolation trenches;

~~wherein planarizing the conformal third layer to form therefrom said upper surface for each said isolation trench that is co-planar to the other said upper surfaces further comprises planarizing said conformal third layer and each said spacer to form therefrom said co-planar upper surfaces, and said planarizing the conformal third layer is performed in the absence of masking the conformal third layer over each of said isolation trenches~~; and

wherein the microelectronic structure is defined at least in part by the plurality of spacers, the conformal third layer, and the plurality of isolation trenches.

19. (Currently Amended) ~~A method~~The method according to Claim 18, wherein ~~said~~the upper surface for each ~~said~~the isolation trench is formed by chemical mechanical planarization.

20. (Currently Amended) ~~A method~~The method according to Claim 18, further comprising forming a doped region below the termination of each ~~said~~the isolation trench within ~~said~~the semiconductor substrate.

21. (Currently Amended) ~~A method~~The method according to Claim 18, further comprising, prior to filling each ~~said~~the isolation trench with ~~said~~the conformal third layer, forming a liner upon a sidewall of each ~~said~~the isolation trench, ~~said~~the liner being confined preferentially within each ~~said~~the isolation trench and extending from an interface thereof with ~~said~~the oxide layer to the termination of ~~said~~the isolation trench within ~~said~~the semiconductor substrate, and wherein ~~said~~the conformal third layer is composed of an electrically insulative material.

22. (Currently Amended) ~~A method~~The method according to Claim 21, wherein ~~said~~the liner is a thermally grown oxide of ~~said~~the semiconductor substrate.

23. (Canceled).

24. (Currently Amended) A method of forming a microelectronic structure, the method comprising:

forming an oxide layer upon a semiconductor substrate;

forming a polysilicon layer upon ~~said~~the oxide layer;

forming a first dielectric layer upon ~~said~~the polysilicon layer;

selectively removing ~~said~~the first dielectric layer and ~~said~~the polysilicon layer to expose ~~said~~the oxide layer at a plurality of areas;

forming a second dielectric layer conformally over ~~said~~the oxide layer, ~~said~~the polysilicon layer, and ~~said~~the first dielectric layer, wherein ~~said~~ forming a second dielectric layer includes forming a second dielectric layer on and in contact with the exposed oxide layer at ~~said~~the plurality of areas;

selectively removing ~~said~~the second dielectric layer to form a plurality of spacers from ~~said~~the second dielectric layer, wherein each ~~said~~ spacer is upon ~~said~~the oxide layer, is in contact with both ~~said~~the polysilicon layer and ~~said~~the first dielectric layer, and is adjacent to an area of sad plurality of areas;

forming a plurality of isolation trenches extending below ~~said~~the oxide layer and from top edges into and terminating within ~~said~~the semiconductor substrate, wherein each ~~said~~ isolation trench of the plurality of isolation trenches is adjacent to and below a pair of ~~said~~the spacers and is situated at a corresponding area of ~~said~~the plurality of areas;

rounding the top edges of each ~~of said~~ isolation trench of the plurality of isolation trenches;

filling each ~~said~~ isolation trench of the plurality of isolation trenches with a conformal third layer, ~~said~~the conformal third layer having a top surface and extending above ~~said~~the oxide layer in contact with a corresponding pair of ~~said~~the spacers, wherein ~~said~~ filling is performed by depositing ~~said~~the conformal third layer, and ~~said~~ depositing is carried out to the extent of filling each ~~said~~ isolation trench and extending over ~~said~~the spacers and over ~~said~~the first dielectric layer;

planarizing the conformal third layer to form therefrom an upper surface for each ~~said~~ isolation trench of the plurality of isolation ~~trench~~ trenches that is co-planar to the other ~~said~~ upper surfaces, wherein ~~said~~ planarizing the conformal third layer is performed directly on the top surface of the conformal third layer in the absence of masking the conformal third layer over each of ~~said~~the isolation trenches;

wherein the conformal third layer is an electrically insulative material that extends continuously between and within ~~said~~the plurality of isolation trenches;

wherein ~~said~~the upper surface for each ~~said~~ isolation trench of the plurality of isolation trenches is formed from ~~said~~the conformal third layer, ~~said~~the spacers, and ~~said~~the first dielectric layer; and

wherein the microelectronic structure is defined at least in part by the plurality of spacers, the conformal third layer, and the plurality of isolation trenches.

25. (Currently Amended) A method of forming a microelectronic structure, the method comprising:

forming an oxide layer upon a semiconductor substrate;

forming a polysilicon layer upon ~~said~~the oxide layer;

forming a first dielectric layer upon ~~said~~the polysilicon layer;

selectively removing ~~said~~the first dielectric layer and ~~said~~the polysilicon layer to expose ~~said~~the oxide layer at a plurality of areas;

forming a second dielectric layer conformally over ~~said~~the oxide layer, ~~said~~the polysilicon layer, and ~~said~~the first dielectric layer, wherein ~~said~~the forming a second dielectric layer includes forming a second dielectric layer on and in contact with the exposed oxide layer at ~~said~~the plurality of areas;

selectively removing ~~said~~the second dielectric layer to form a plurality of spacers from ~~said~~the second dielectric layer, wherein each ~~said~~ spacer of the plurality of spacers is upon ~~said~~the oxide layer, is in contact with both ~~said~~the polysilicon layer and ~~said~~the first dielectric layer, and is adjacent to an area of ~~said~~the plurality of areas;

forming a plurality of isolation trenches extending below ~~said~~the oxide layer and from top edges into and terminating within ~~said~~the semiconductor substrate, wherein each ~~said~~ isolation trench of the plurality of isolation trenches is adjacent to and below a pair of ~~said~~the spacers and is situated at a corresponding area of ~~said~~the plurality of areas;

rounding the top edges of each of ~~said~~the isolation trenches;

filling each ~~said~~ isolation trench with a conformal third layer, ~~said~~the conformal third layer having a top surface and extending above ~~said~~the oxide layer in contact with a corresponding pair of ~~said~~the spacers, wherein ~~said~~ filling is performed by depositing ~~said~~the conformal third layer, and ~~said~~ depositing is carried out to the extent of filling each ~~said~~ isolation trench and extending over ~~said~~the spacers and over ~~said~~the first dielectric layer;

planarizing the conformal third layer to form therefrom an upper surface for each ~~said~~ isolation trench that is co-planar to the other ~~said~~the upper surfaces, wherein ~~said~~ planarizing the conformal third layer is performed directly on the top surface of the conformal third layer and in the absence of masking the conformal third layer over each of ~~said~~the plurality of isolation trenches;

exposing ~~said~~the oxide layer upon a portion of a surface of ~~said~~the semiconductor substrate;

forming a gate oxide layer upon ~~said~~the portion of ~~said~~the surface of ~~said~~the semiconductor substrate;

forming between ~~said~~ the plurality of isolation trenches, and confined in the space therebetween, a layer composed of polysilicon upon ~~said~~the oxide layer in contact with a pair of ~~said~~the spacers; and

selectively removing ~~said~~the third layer, ~~said~~the spacers and ~~said~~the layer composed of polysilicon to form a portion of at least one of ~~said~~the upper surfaces;

wherein a material that is electrically insulative extends continuously between and within ~~said~~the plurality of isolation trenches.

26. (Currently Amended) A method of forming a microelectronic structure, the method comprising:

forming an oxide layer upon a semiconductor substrate;

forming a polysilicon layer upon ~~said~~the oxide layer;

forming a first dielectric layer upon ~~said~~the polysilicon layer;

selectively removing ~~said~~the first dielectric layer and ~~said~~the polysilicon layer to expose ~~said~~the oxide layer at a plurality of areas;

forming a second dielectric layer conformally over ~~said~~the oxide layer, ~~said~~the polysilicon layer, and ~~said~~the first dielectric layer, wherein ~~said~~the forming a second dielectric layer includes forming a second dielectric layer on and in contact with the exposed oxide layer at ~~said~~the plurality of areas;

selectively removing ~~said~~the second dielectric layer to form a plurality of spacers from ~~said~~the second dielectric layer, wherein each ~~said~~ spacer of the plurality of spacers is upon ~~said~~the oxide layer, is in contact with both ~~said~~the polysilicon layer and ~~said~~the first dielectric layer, and is adjacent to an area of ~~said~~the plurality of areas;

forming a plurality of isolation trenches extending below ~~said~~the oxide layer and from top edges into and terminating within ~~said~~the semiconductor substrate, wherein each ~~said~~ isolation trench of the plurality of isolation trenches is adjacent to and below a pair of ~~said~~the spacers and is situated at a corresponding area of ~~said~~the plurality of areas;

rounding the top edges of each isolation trench of ~~said~~the plurality of isolation trenches;

filling each ~~said~~ isolation trench with a conformal third layer, ~~said~~the conformal third layer extending above ~~said~~the oxide layer in contact with a corresponding pair of ~~said~~the spacers, wherein ~~said~~ filling is performed by depositing ~~said~~the conformal third layer, and ~~said~~ depositing is carried out to the extent of filling each ~~said~~ isolation trench and extending over ~~said~~the spacers and over ~~said~~the first dielectric layer;

planarizing the conformal third layer in a single-step by an etch using an etch recipe that etches ~~said~~the conformal third layer and the spacers faster than the first dielectric ~~layer faster than said conformal third layer and said spacers~~ by a ratio in a range from of about 1:1 to about 2:1 to form therefrom an upper surface for each ~~said~~ isolation trench that is co-planar to the other ~~said~~ upper surfaces, wherein ~~said~~ planarizing the conformal third layer is performed in the absence of masking the conformal third layer over each of ~~said~~the isolation trenches;

wherein a material that is electrically insulative extends continuously between and within ~~said~~the plurality of isolation trenches; and

wherein the microelectronic structure is defined at least in part by the plurality of spacers, the conformal third layer, and the plurality of isolation trenches.

27. (Currently Amended) A method according to Claim 26, wherein ~~said~~the ratio is in a range from about 1.3:1 to about 1.7:1.

28-30 (Canceled).

31. (Currently Amended) A method of forming a microelectronic structure, the method comprising:

forming a pad oxide layer upon a semiconductor substrate;

forming a polysilicon layer upon ~~said~~the oxide layer;

forming a silicon nitride layer upon ~~said~~the polysilicon layer;

selectively removing ~~said~~the silicon nitride layer and ~~said~~the polysilicon layer to expose ~~said~~the oxide layer at a plurality of areas;

forming a first silicon dioxide layer over ~~said~~the oxide layer and over ~~said~~the silicon nitride layer, wherein ~~said~~the forming a first silicon dioxide layer includes forming a first silicon dioxide layer on and in contact with the exposed oxide layer at ~~said~~the plurality of areas;

selectively removing ~~said~~the first silicon dioxide layer to form a plurality of spacers from ~~said~~the first silicon dioxide layer, wherein each ~~said~~ spacer of the plurality of spacers is situated upon ~~said~~the oxide layer, is in contact with ~~said~~the silicon nitride layer and ~~said~~the polysilicon layer, and is adjacent to an area of ~~said~~the plurality of areas;

forming a plurality of isolation trenches extending below ~~said~~the oxide layer and from top edges into and terminating within ~~said~~the semiconductor substrate, wherein each ~~said~~ isolation trench of the plurality of isolation trenches is adjacent to and below a pair of ~~said~~the spacers and is situated at a corresponding area of ~~said~~the plurality of areas;

forming a corresponding doped region below the termination of each ~~said~~ isolation trench within ~~said~~the semiconductor substrate;

forming a liner upon a sidewall of each ~~said~~ isolation trench, each ~~said~~ liner extending from an interface thereof with ~~said~~the oxide layer to the termination of ~~said~~the isolation trench within ~~said~~the semiconductor substrate;

rounding the top edges of ~~said~~the isolation trenches;

filling each ~~said~~ isolation trench with a conformal second layer, ~~said~~the second layer extending above ~~said~~the oxide layer in contact with a corresponding pair of ~~said~~the spacers, wherein ~~said~~ filling is performed by depositing ~~said~~the conformal second layer, and ~~said~~ depositing is carried out to the extent of filling each ~~said~~ isolation trench and extending over ~~said~~the spacers and over ~~said~~the silicon nitride layer; and

planarizing ~~said~~the conformal second layer and each of ~~said~~the spacers to form therefrom an upper surface for each ~~said~~ isolation trench that is co-planar to the other ~~said~~ upper surfaces and is situated above ~~said~~the oxide layer, wherein ~~said~~ planarizing is performed in a single-step and in the absence of masking the conformal second layer over each of ~~said~~the isolation trenches;

wherein a material that is electrically insulative extends continuously between and within ~~said~~the plurality of isolation trenches.

32. (Currently Amended) ~~A method~~The method according to Claim 31, wherein each ~~said~~the liner is a thermally grown oxide of ~~said~~the semiconductor substrate, and wherein ~~said~~the conformal second layer is composed of an electrically insulative material.

33. (Currently Amended) ~~A method~~The method according to Claim 31, wherein each ~~said~~the liner is composed of silicon nitride, and wherein ~~said~~the conformal second layer is composed of an electrically insulative material.

34. (Currently Amended) ~~A method~~The method according to Claim 31, further comprising:

exposing ~~said~~the oxide layer upon a portion of a surface of ~~said~~the semiconductor substrate;

forming a gate oxide layer upon ~~said~~the portion of ~~said~~the surface of ~~said~~the semiconductor substrate;

forming between ~~said~~said the plurality of isolation trenches, and confined in the space therebetween, a layer composed of polysilicon upon ~~said~~the gate oxide layer in contact with a pair of ~~said~~the spacers, and

selectively removing ~~said~~the layer composed of polysilicon to form a portion of at least one of ~~said~~the upper surfaces.

35. (Currently Amended) A method for forming a microelectronic structure, the method comprising:

providing a semiconductor substrate having a top surface with an oxide layer thereon;

forming a polysilicon layer upon ~~said~~the oxide layer;

forming a first layer upon ~~said~~the polysilicon layer;

selectively removing ~~said~~the first layer and ~~said~~the polysilicon layer to expose ~~said~~the oxide layer at a plurality of areas;

forming a plurality of isolation trenches through the exposed oxide layer at ~~said~~the plurality of areas, wherein an electrically insulative material extends continuously between and within ~~said~~the plurality of isolation trenches, each ~~said~~ isolation trench:

having a spacer composed of a dielectric material upon ~~said~~the oxide layer in contact with ~~said~~the first layer and ~~said~~the polysilicon layer;

extending from an opening thereto at the top surface of ~~said~~the semiconductor substrate and below ~~said~~the oxide layer into and terminating within ~~said~~the semiconductor substrate adjacent to and below ~~said~~the spacer;

having a second layer including a top surface and filling ~~said~~the isolation trench and extending above ~~said~~the oxide layer in contact with ~~said~~the spacer, wherein ~~said~~ filling is performed by depositing ~~said~~the second layer, and ~~said~~ depositing is carried out to the extent of filling each ~~said~~ isolation trench and extending over ~~said~~the spacer and over ~~said~~the first layer;

having a top edge and ~~said~~the top edge being rounded; and

having a planar upper surface formed from ~~said~~the second layer and ~~said~~the spacer and being situated above ~~said~~the oxide layer, wherein ~~said~~the planar upper surface is formed by planarizing the top surface of the second layer in the absence of masking ~~said~~the second layer over each of ~~said~~the isolation trenches; and

wherein the microelectronic structure is defined at least in part by the plurality of spacers, the second layer, and the plurality of isolation trenches.

36. (Currently Amended) The method as defined in Claim 35, further comprising:

doping the semiconductor substrate with a dopant having a first conductivity type;

doping the semiconductor substrate below each ~~said~~ isolation trench with a dopant having a second conductivity type opposite the first conductivity type to form a doped trench bottom that is below and in contact with a respective one of each ~~said~~the isolation trench.

37. (Currently Amended) The method as defined in Claim 36, wherein the doped trench bottom has a width, each ~~said~~ isolation trench has a width, and the width of each ~~said~~ doped trench bottom is greater than the width of the respective isolation trench.

38. (Currently Amended) A method for forming a microelectronic structure, the method comprising:

providing a semiconductor substrate having a top surface with an oxide layer thereon;

forming a first layer upon ~~said~~the oxide layer;

selectively removing ~~said~~the first layer to expose ~~said~~the oxide layer at a plurality of areas;

forming a plurality of isolation trenches through the oxide layer at ~~said~~the plurality of areas, wherein an electrically insulative material extends continuously between and within ~~said~~the plurality of isolation trenches, each ~~said~~ isolation trench:

having a spacer composed of a dielectric material upon ~~said~~the oxide layer in contact with ~~said~~the first layer;

extending from an opening thereto at the top surface of ~~said~~the semiconductor substrate and below ~~said~~the oxide layer into and terminating within ~~said~~the semiconductor substrate adjacent to and below ~~said~~the spacer;

having a second layer filling ~~said~~the isolation trench and extending above ~~said~~the oxide layer in contact with ~~said~~the spacer, wherein ~~said~~the filling is performed by depositing ~~said~~the second layer, and ~~said~~the depositing is carried out to the extent of filling each ~~said~~the isolation trench and extending over ~~said~~the spacer and over ~~said~~the first layer;

having a top edge and ~~said~~the top edge being rounded; and

having a planar upper surface formed from ~~said~~the second layer and ~~said~~the spacer and being situated above ~~said~~the oxide layer, wherein ~~said~~the planar upper surface is formed by directly planarizing the second layer in the absence of masking ~~said~~the second layer over each of ~~said~~the isolation trenches; and

wherein the microelectronic structure is defined at least in part by the plurality of spacers, the second layer, and the plurality of isolation trenches.

39. (Currently Amended) The method as defined in Claim 38, further comprising:

doping the semiconductor substrate with a dopant having a first conductivity type; and

doping the semiconductor substrate below each ~~said~~ isolation trench with a dopant having a second conductivity type opposite the first conductivity type to form a doped trench bottom that is below and in contact with a respective one of ~~said~~<u>the</u> isolation trenches.

40. (Currently Amended) The method as defined in Claim 39, wherein:

the doped trench bottom has a width;

each ~~said~~ isolation trench has a width; and the width of each ~~said~~ doped trench bottom is greater than the width of the respective isolation trench.

41. (Canceled).

42. (Currently Amended) A method for forming a microelectronic structure, the method comprising:

providing a semiconductor substrate having a top surface with an oxide layer thereon;

forming a polysilicon layer upon ~~said~~<u>the</u> oxide layer; forming a first layer upon ~~said~~<u>the</u> polysilicon layer;

forming a first isolation structure including:

a first spacer composed of a dielectric material upon ~~said~~<u>the</u> oxide layer in contact with ~~said~~<u>the</u> first layer and ~~said~~<u>the</u> polysilicon layer;

a first isolation trench extending from an opening thereto at top edges at the top surface of ~~said~~the semiconductor substrate and below ~~said~~the oxide layer into and terminating within ~~said~~the semiconductor substrate adjacent to and below ~~said~~the first spacer, wherein ~~said~~the first spacer is situated on a side of ~~said~~the first isolation trench, and wherein ~~said~~the first isolation trench has a top edge that is rounded; and

a second spacer composed of a dielectric material upon ~~said~~the oxide layer in contact with ~~said~~the first layer and ~~said~~the polysilicon layer, ~~said~~the second spacer being situated on a side of ~~said~~the first isolation trench opposite the side of ~~said~~the first spacer;

forming a second isolation structure including:

a first spacer composed of a dielectric material upon ~~said~~the oxide layer in contact with ~~said~~the first layer and ~~said~~the polysilicon layer;

a first isolation trench extending from an opening thereto at top edges at the top surface of ~~said~~the semiconductor substrate and below ~~said~~the oxide layer into and terminating within ~~said~~the semiconductor substrate adjacent to and below ~~said~~the first spacer of ~~said~~the second isolation structure, wherein ~~said~~the first spacer of ~~said~~the second isolation structure is situated on a side of ~~said~~the first isolation trench, and wherein ~~said~~the first isolation trench in ~~said~~the second isolation structure has a top edge that is curved; and

a second spacer composed of a dielectric material upon ~~said~~the oxide layer in contact with ~~said~~the first layer and ~~said~~the polysilicon layer, ~~said~~the second spacer of ~~said~~the second isolation structure being situated on a side of ~~said~~the first isolation trench opposite the side of ~~said~~the first spacer of ~~said~~the second isolation structure;

rounding the top edges of ~~said~~the isolation trenches;

forming an active area located within ~~said~~the semiconductor substrate between ~~said~~the first and second isolation structures;

forming a conformal second layer, composed of an electrically insulative material, filling ~~said~~the first and second isolation trenches and extending continuously therebetween and above ~~said~~the oxide layer in contact with ~~said~~the first and second spacers of ~~said~~the respective first and second isolation structures, wherein ~~said~~ filling is performed by depositing ~~said~~the conformal second layer, and ~~said~~ depositing is carried out to the extent of filling each of ~~said~~the isolation trenches and extending over ~~said~~the spacers and over ~~said~~the first layer; and

forming with a single etch recipe in the absence of a mask a planar upper surface from ~~said~~the conformal second layer and ~~said~~the first and second spacers of ~~said~~the respective first and second isolation structures, and being situated above ~~said~~the oxide layer;

wherein the microelectronic structure is defined at least in part by the active area, the second layer, and the first and second isolation trenches.

43. (Currently Amended) A method for forming a microelectronic structure, the method comprising:

providing a semiconductor substrate having a top surface with an oxide layer thereon;

forming a first layer upon ~~said~~the oxide layer;

forming a first isolation structure including:

a first spacer composed of a dielectric material upon ~~said~~the oxide layer in contact with ~~said~~the first layer;

a first isolation trench extending from an opening thereto at the top surface of ~~said~~the semiconductor substrate and below ~~said~~the oxide layer into and terminating within ~~said~~the semiconductor substrate adjacent to and below ~~said~~the first spacer, wherein ~~said~~the first spacer is situated on a side of ~~said~~the first isolation trench, and wherein ~~said~~the first isolation trench has a top edge that is rounded; and

a second spacer composed of a dielectric material upon ~~said~~the oxide layer in contact with ~~said~~the first layer, ~~said~~the second spacer being situated on a side of ~~said~~the first isolation trench opposite the side of ~~said~~the first spacer;

forming a second isolation structure including:

a first spacer composed of a dielectric material upon ~~said~~the oxide layer in contact with ~~said~~the first layer;

a first isolation trench extending below ~~said~~the oxide layer into and terminating within ~~said~~the semiconductor substrate adjacent to and below ~~said~~the first spacer of ~~said~~the second isolation structure, wherein ~~said~~the first spacer of ~~said~~the second isolation structure is situated on a side of ~~said~~the first isolation trench, and wherein ~~said~~the first isolation trench in ~~said~~the second isolation structure has a top edge that is rounded; and

a second spacer composed of a dielectric material upon ~~said~~the oxide layer in contact with ~~said~~the first layer, ~~said~~the second spacer of ~~said~~the second isolation structure being situated on a side of ~~said~~the first isolation trench opposite the side of ~~said~~the first spacer of ~~said~~the second isolation structure;

forming an active area located within ~~said~~the semiconductor substrate between ~~said~~the first and second isolation structures;

forming a conformal second layer having a top surface, composed of an electrically insulative material, conformally filling ~~said~~the first and second isolation trenches and extending continuously therebetween and above ~~said~~the oxide layer in contact with ~~said~~the first and second spacers of ~~said~~the respective first and second isolation structures, wherein ~~said~~ filling is performed by depositing ~~said~~the conformal second layer, and ~~said~~ depositing is carried out to the extent of filling each of ~~said~~the isolation trenches and extending over ~~said~~the spacers and over ~~said~~the first layer; and

planarizing the conformal second layer and ~~said~~the first and second spacers of ~~said~~the respective first and second isolation structures to form a planar upper surface from ~~said~~the conformal second layer and ~~said~~the first and second spacers of ~~said~~the respective first and second isolation structures, and being situated above ~~said~~the oxide layer, wherein ~~said~~the planarizing is performed directly on the top surface of the conformal second layer in the absence of masking the conformal second layer over each of ~~said~~the isolation trenches, and wherein the microelectronic structure is defined at least in part by the active area, the conformal second layer, and the first and second isolation trenches.